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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Application Number: 10/616,341
Filing Date: July 09, 2003
Appellant(s): DAY ET AL.

William N. Hogg
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 26, 2006 appealing from the Office action mailed May 19, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the Brief is substantially correct. The summary failed to specifically identify that claim 1 is the only independent claim to which the invention pertains (which was specifically discussed with reference to page and line numbers as well as the Figures of the specification in the summary of the claimed subject matter contained in the Brief).

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

(A) Listing of Evidence Relied Upon

2000-68620	Nakaya et al (Japan)	3-3-2000
5,401,913	Gerber et al	3-28-1995

The appellant's admitted prior art as described on pages 1-2 of the specification.

(B) Brief Description of Evidence Relied Upon

The **admitted prior art** suggested that those skilled in the art of making conventional printed wiring boards for such things as high frequency applications desired to provide adequate adhesion between the copper and dielectric laminate and provided the same via an operation wherein the initially smooth surfaces of the wiring and voltage planes are made rough to promote adhesion (where such roughening techniques included oxide replacement processes as well as application of brass, zinc or nickel on the copper surface to all of the exposed surface of the copper prior to personalization as well as after personalization of the copper plane (presumably personalized via an etching operation). The admitted prior art did not envision the roughening of only selected regions of the copper in order to allow for the remaining regions to retain a smooth surface for improved conductivity in the assembly.

Japanese Patent '620 suggested that in the art of manufacturing a printed circuit board it was known at the time the invention was made to roughen only the regions of the lands in the copper circuit pattern as such roughening would have increased the bond between the conductive material of the through hole and the copper layer as well as improved adhesion between the adhesive of the conductive material and the copper

layer. The reference to Japanese Patent '620 additionally suggested that only roughening the land regions would have allowed one to provide finer patterns via etching of the copper surface (personalizing it in finer detail was possible because those areas which were not roughened were easier to pattern via etching).

Gerber et al taught that it was known to employ an epoxy resin impregnated material as a dielectric material between conductive layers in a multilayer printed circuit board.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art in view of Japanese Patent 2000-68620 and Gerber et al (all newly cited).

The admitted prior art as characterized on pages 1-2 of the specification made it clear that in the formation of printed wiring boards it was known at the time the invention was made to form the same via a laminating operation which included the step of roughening the entire surface of the substrates to be laminated with the dielectric material in order to provide adequate adhesion between the copper and the dielectric in the laminated structure. Typically prior to the lamination operation the surfaces of the substrates are smooth and they are roughened along their entire surface in order to promote adhesion. The conventional known roughening the surface prior to the lamination operation included oxide and oxide replacement processes as well as the application of brass, zinc, or nickel onto the copper surface. Thus, it was known prior to

lamination to roughen the surface of the substrate including the copper over the entirety of the surface of the substrate and that prior to the roughening operation the substrate surfaces were known to have been smooth. The admitted prior art failed to teach the selective roughening of the signal plane which did not include all of the signal plane but rather included the lands on the surface of the same and that the lamination operation was performed with a sticker sheet (a dielectric film or ply formed from epoxy and fiberglass material, i.e. a prepreg for example).

However, in order to facilitate the formation of fine lines in the circuit pattern of a substrate in a printed circuit board, it was known at the time the invention was made to roughen only the surface of the land regions where the through holes were to be formed and to not roughen the other areas of the copper layer of the assembly as such allowed for formation of a fine circuit patterns in the copper foil as evidenced by Japanese Patent '620. The reference to Japanese Patent '620 additionally suggested that the roughening of the substrate at the land regions resulted in better conductive contact at the through hole regions. Japanese Patent '620 expressly stated that better conductivity was obtained as well as better adhesion between the adhesive material which made up part of the conductive material filling the through hole. Applicant is more specifically referred to paragraphs [0011]-[0012] and [0065]. Note that the regions of the lands of the copper layer 3 are roughened where the through hole was to be formed while the other regions of the copper layer 3 were not roughened. It should be noted that copper layers 3 were disposed adjacent each other with a dielectric material 1 disposed there

between. The references failed to expressly teach that it was known to employ a sticker sheet in the lamination of the layers together in the manufacture of the circuit board.

The reference to Gerber clearly expressed that it was known at the time the invention was made to employ a sticker sheet to join the conductive substrates together wherein the sticker sheet was formed from a dielectric material. More specifically, Gerber suggested that it was known to apply an adhesive film 58, 24, 60, and 62 to join the layers of the multilayer board together. The reference suggested that the adhesive was in the form of a film layer, see the abstract of the disclosure and column 5, lines 44-46 for example and additionally suggested that the adhesive layers were electrically insulative, see column 5, lines 44-46, column 5, lines 58-63. It should also be noted that the reference to Gerber et al suggested that epoxy was useful as the adhesive material in the layers 58, 24, 60 and 62. Clearly, the use of an adhesive sticker sheet which was a dielectric adhesive layer was known to assembly of plural layers in the lamination of a multilayer printed circuit board. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a sticker sheet to join plural layers of a multilayer assembly of a circuit board formed via lamination as suggested by Gerber (note that the admitted prior art suggested that the boards were formed via lamination and Gerber is just evidencing that which was conventionally known at the time the invention was made as a suitable manner for lamination of the layers together in a multilayer board) wherein one only roughened the surface of the lands of the copper foil of the substrate where a through hole was to be formed as such would have allowed for finer circuit patterns in the remainder of the copper layer as suggested by Japanese

Patent 2000-68620 (as well as improved electrical contact in the area where the through holes were provided) in the process of making a multilayer circuit board as taught by the appellant's admitted prior art.

With regard to claims 3-5, 8, and 9, the appellant is advised that the admitted prior art appears to suggest that the surfaces of the layers are smooth having a roughness of less than 1 R_z when no roughening operation was performed and that in the typical roughening operation of the prior art the roughness appeared to have been greater than 3 R_z. the roughening of the surface appears to have been to promote better adhesion of the layers and one would have understood that roughness greater than 3 R_z would have provided for the same. Additionally the reference to Japanese Patent '620 clearly roughened the surface in order to ensure a tight assembly at the land region which was subjected to through hole formation. The specific degree of roughening would have been determined through routine experimentation and would have included use of the conventional roughening techniques (the same techniques employed by appellant) in order to provide adequate contact of the plies as well as avoidance of roughness in those regions where fine circuitry was desired in accordance with Japanese Patent '620. Regarding claims 6 and 7, the appellant is advised that the reference suggested that there were several lands which were roughened in each layer of the assembly, see the Figures of the reference wherein the surfaces included at least three lands. Additionally, note that the reference suggested that adjacent layers would have been roughened in order to facilitate joinder in the land region. The use of roughening of both the signal layer and the voltage plane in only selective regions

therein would have been understood in light of the teachings of the reference to Japanese Patent '620 to have been performed in the processing therein. With respect to claims 10-15, one skilled in the art would have understood how to utilize a mask to prevent roughening in those regions where it was undesirable. Additionally, the specified roughening techniques of plating and or oxide or an oxide replacement process were known to those skilled in the art at the time the invention was made and admitted by appellant as known for the purpose of roughening the layer in circuit board manufacture. The specific manner that one roughened the surface is taken as well known in the art and additionally the use of a photoresist in the operation is likewise taken as conventional in the art. One skilled in the art would have been expected to utilize the known techniques for roughening in order to perform the selective roughening of the substrate as taught by Japanese Patent '620.

(10) Response to Argument

Regarding the patentability of the independent claim (claim 1), the appellant essentially has two arguments for the patentability of the claim: (1) none of the prior art taught the use of a sticker sheet to form the composite structure wherein the sticker sheet is a dielectric material which was disposed between signal lines and a voltage plane (noting the Gerber did not teach a voltage plane), and; (2) the reference to Japanese patent '620 was performing the operation of roughening in order to render the conductive filled through holes have a superior electrical contact and not for the purpose of imparting improved adhesion between the copper and dielectric material of the sticker

sheet (and thus there is not a satisfactory reason to make the combination as proposed by the examiner). These reasons are respectfully traversed.

First regarding the use of a sticker sheet, the appellant refers one to page 7, lines 20-22 of the specification for discussion of what a "sticker sheet" is (i.e. that the sticker sheet is a dielectric material). Page 7 lines 20-22 of the specification states:

> "The sticker sheet also preferably is made of FR4 material and is maintained in the B cured state (partially cured) for lamination, after which the laminate is fully cured."

The above quoted passage does not state the sticker sheet material is dielectric, however at page 7, lines 12-13, the specification states:

> "The reference voltage layer 12 has a copper voltage plane 26 laminated to a dielectric material 27 which again, preferably is FR4."

Thus, the FR4 material can be said to be a dielectric material. That said, appellant's specification additionally states at page 6, lines 15-17 that:

> FR4 material is an epoxy coated fiberglass material well known in the art and can be laminated, if one of the laminates is in the partially cured condition and then fully cured."

Thus it can be ascertained from the specification that FR4 is a dielectric material which was well known in the art and which was a fiberglass material which was coated with epoxy. The reference to Gerber et al employed electrically insulating (i.e. dielectric) bonding film layers 58, 24, 60, and 62 between circuit layers 26, 10, 28, and 30 where the polymer of choice was an epoxy compound, column 5, lines 44-63. The use of a conductive film in Gerber et al (column 6, lines 32-57) which appears to be referenced by appellant relates to an alternative embodiment (not the embodiment referred to in the

Office action). Additionally electrically insulating epoxy layers like FR4 were well known in the art as expressed by appellant. As to the lack of a voltage plane in Gerber, the admitted prior art expressed the lamination of the layer having the signal lines to the voltage plane in the manufacture of a circuit board (presumably with a dielectric material otherwise the board would short out) and the reference to Gerber et al clearly related to circuit board manufacture which was conventionally practiced. One skilled in the art would have understood that in the process of the admitted prior art the known FR4 would have been used to laminate the layers together as the reference to Gerber clearly suggested lamination of layers of a circuit board with epoxy resin film layers (which is what FR4 was) and such FR4 was well known in the art as expressed by appellant in the specification.

Regarding the second argument for patentability of the claims, namely that the reference to Japanese Patent '620 performed the roughening only to improve electrical contact and that this has nothing to do with why appellant performed the roughening only in selected zones, the appellant is advised initially that the claims at hand do not establish in any shape or form the nexus between the roughening of the selected regions and the improved adhesion in the finished assembly. Nor is there any nexus in the claim between the reductions in conductive losses for the signal because the regions outside of the lands are not roughened. In other words, the claim as presented is not commensurate in scope with the appellant's arguments. That said, the appellant is advised that the reference to Japanese Patent '620 provided for roughening only in

select regions like the lands in order to not only improve the conductive contact but also to improve adhesive strength as expressed in paragraph [0011] of the reference:

> "[0011] Because the contact interface between the conductive composition and the wiring pattern is coarsened in the first configuration, the contact area is increased, the number of contact points between the conductive filler in the conductive composition and the wiring pattern is increased, the adhesive strength between the resin in the conductive composition and the wiring pattern is increased and the connect reliability is improved."

Japanese Patent '620 goes on to state in paragraph [0012] that the use of the roughening in the selected regions allowed for easier precision pattern formation in the circuit patterning:

> "[0012] Because the coarsened region of the wiring pattern is limited to the connection interface with the conductive composition in the first configuration, fine pattern formation in the wiring pattern is easier than when the entire surface is coarsened. In circuit boards where fully coarsened metal foil is laminated on an insulating layer, the coarsened portion has to be deeply embedded in the insulating layer when the metal foil is etched for circuit pattern formation. This requires over etching, which makes improved pattern precision difficult."

Clearly, Japanese Patent '620 provided for roughening only selected regions like the lands of the layers in order to provide for better pattern formation in the circuitry of the boards as well as improving the electrical contact in the through hole regions as well as enhanced adhesion between the adhesive of the conductive material in the through hole regions and the metal surfaces of the board. While the reference did not express that the roughening of the selected regions provided for improved adhesion between the dielectric layer and the metal layer of the laminate while not impairing the conductivity of the signal (i.e. increasing the conductive losses which results from roughening the entire surface), the reference need not express the identified benefits in order to render the claimed invention obvious. Moreover, one skilled in the art would have been directed to

selectively roughen the copper layer in the region of the lands in order to allow for better circuitry formation as well as to improve electrical and adhesive contact between the layers of the board in the regions of the land as suggested by Japanese Patent '620 and the fact that appellant chose to selectively roughen the layer for a different reason does not alter the conclusion that it would have been prima facie obvious to perform the specified roughening for the reasons identified by the reference, see In re Shetty, 195 USPQ 753, In re Hoch, 166 USPQ 406, In re Wilder, 166 USPQ 545 and In re Lintner, 173 USPQ 360. Thus, while it appears that the reference performed the roughening for a different purpose, it would have nonetheless been obvious to perform the same for the specified reasons identified. Additionally, it should be noted that the admitted prior art recognized that roughening the entire surface was desirable in order to improve adhesion presumably between the metal layers and the dielectric layers. As Japanese Patent '620 expressed increased adhesion between the adhesive of the conductive material and the metal layer with the selective roughening, one skilled in the art would have understood that there likewise would have been improved adhesion between the metal and the dielectric material in the processing of the admitted prior art where only selective roughening in accordance with Japanese Patent '620 was performed. The fact that Japanese Patent only selectively roughened and yet achieved adequate adhesion evidenced that such would have been attained when practicing the identified roughening operation. Thus, appellant's second argument regarding the specific need for the prior art reference to identify the same problem with a similar solution has not been found to be persuasive.

There clearly is motivation as set forth in Japanese Patent '620 to modify the admitted prior art to only selectively roughen the copper layer of the substrate in the land regions prior to lamination of the layers in order to obtain the benefits expressly described by Japanese Patent '620. The fact that appellant does not desire to achieve these specified benefits does not alter the conclusion that it would have been obvious to perform the selective roughening for the reasons specified. Additionally as noted above, the references to the admitted prior art as well as Gerber et al suggested the use of a sticker sheet which was in fact a dielectric material.

Regarding the rejection of claims 3-15 the appellant argues that these claims all depend from claim 1 and thus are allowable for the same reasons as noted in the brief. However, as expressed above these reasons identified by appellant have not been found to be persuasive and therefore the rejection of claims 3-15 should be sustained. More specifically regarding claims 3-5, the appellant argues that there is no art which suggested the degree of roughness or smoothness of the signal plane and there is no indication that the choices made by appellant were desirable or even appropriate. This has not been found to be persuasive. As noted above, the admitted prior art appears to suggest that the surfaces of the layers are smooth having a roughness of less than 1 R_z when no roughening operation was performed and that in the typical roughening operation of the prior art the roughness appeared to have been greater than 3 R_z. The roughening of the surface appears to have been to promote better adhesion of the layers and one would have understood that roughness greater than 3 R_z would have provided for the same. Note that use of conventional roughening techniques appear to

provide for this conventional roughening. Additionally the reference to Japanese Patent '620 clearly roughened the surface in order to ensure a tight assembly at the land region which was subjected to through hole formation. The specific degree of roughening would have been determined through routine experimentation and would have included use of the conventional roughening techniques (the same techniques employed by appellant) in order to provide adequate contact of the plies as well as avoidance of roughness in those regions where fine circuitry was desired in accordance with Japanese Patent '620. Note that appellant was advised of the same in the final rejection and has not properly traversed the same other than to state that there is no evidence from the prior art and no indication that these choices were desirable or appropriate. However, the selection of the degree of roughness (for a smooth surface having a roughness of less than 1 R_z and for a rough surface a roughness greater than 3 R_z) is nothing more than provision of that which the admitted prior art suggested was provided fro the smooth or rough regions. Claims 3-5 stand rejected for the reasons identified above.

Regarding claims 8, 9, and 13-15, the appellant argues that there is no suggestion of a voltage plane related to the signal plane. However, as noted above, the admitted prior art clearly suggested that there was a voltage plane used in combination with the signal plane in the manufacture of a circuit board assembly. Appellant's argument to the contrary is not understood since the admitted prior art clearly included the use of a voltage plane. Additionally appellant argues that because the art failed to teach the specified voltage plane it must have therefore failed to teach the suggested

roughened and smooth areas of the same as recited in claim 9. However as previously noted above the roughening of selected regions throughout the board assembly was clearly suggested by Japanese Patent '620. To selectively roughen the land regions of the signal lines and the specified regions of the voltage plane would have been obvious in light of Japanese patent '620 for the reasons previously noted. Appellant's arguments to the contrary have not been found to be persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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